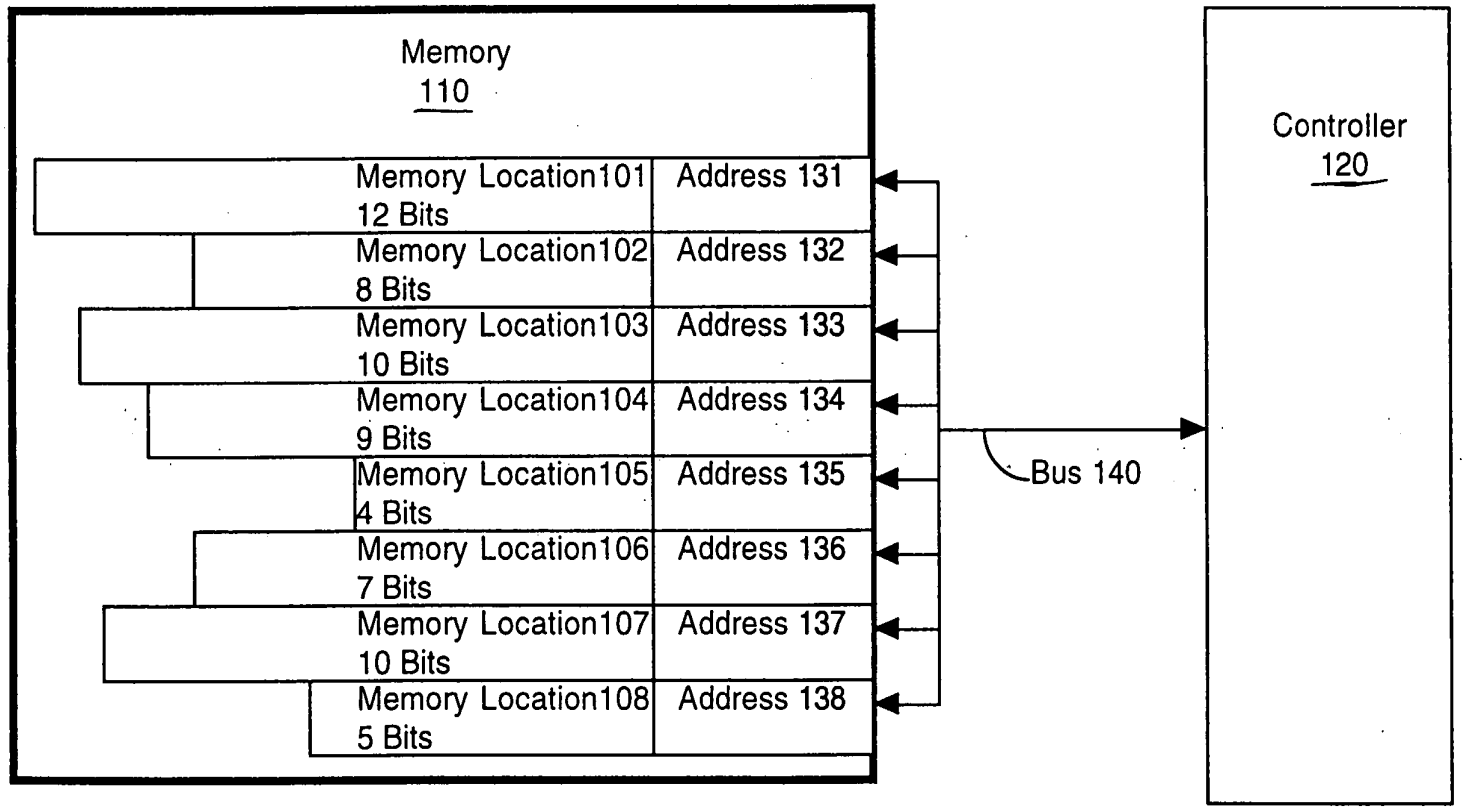
100
Memory
110
Memory Location101
12 Bits
Address 131
Memory Location102
8 Bits
Address 132
Memory Location103
10 Bits
Address 133
Memory Location104
9 Bits
Address 134
Memory Location105
4 Bits
Address 135
Memory Location106
7 Bits
Address 136
Memory Location107
10 Bits
Address 137
Memory Location108
5 Bits
Address 138
Bus 140
Controller
120

FIG 1

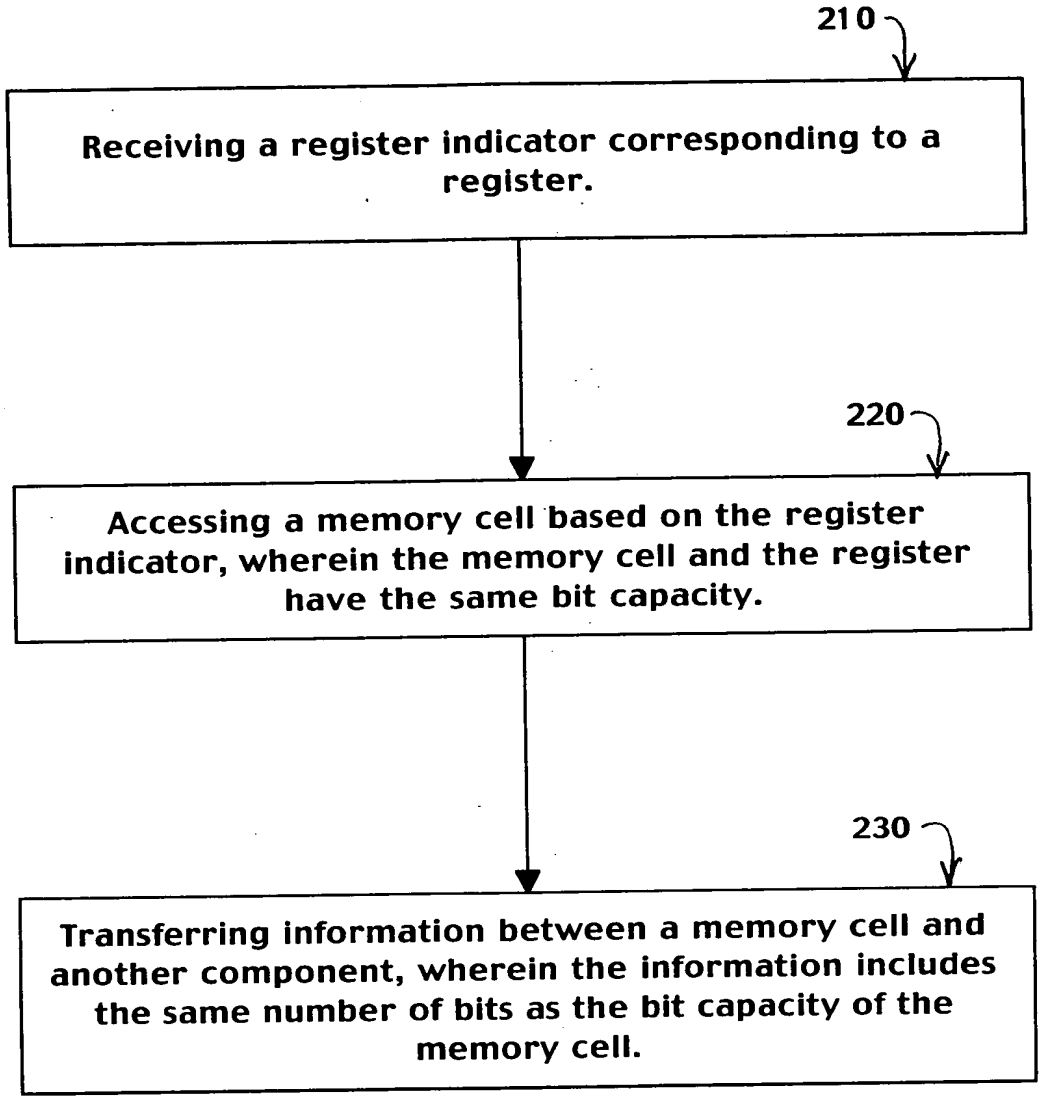
200
210
Receiving a register indicator corresponding to a register.
220
Accessing a memory cell based on the register indicator, wherein the memory cell and the register have the same bit capacity.
230
Transferring information between a memory cell and another component, wherein the information includes the same number of bits as the bit capacity of the memory cell.

FIG 2

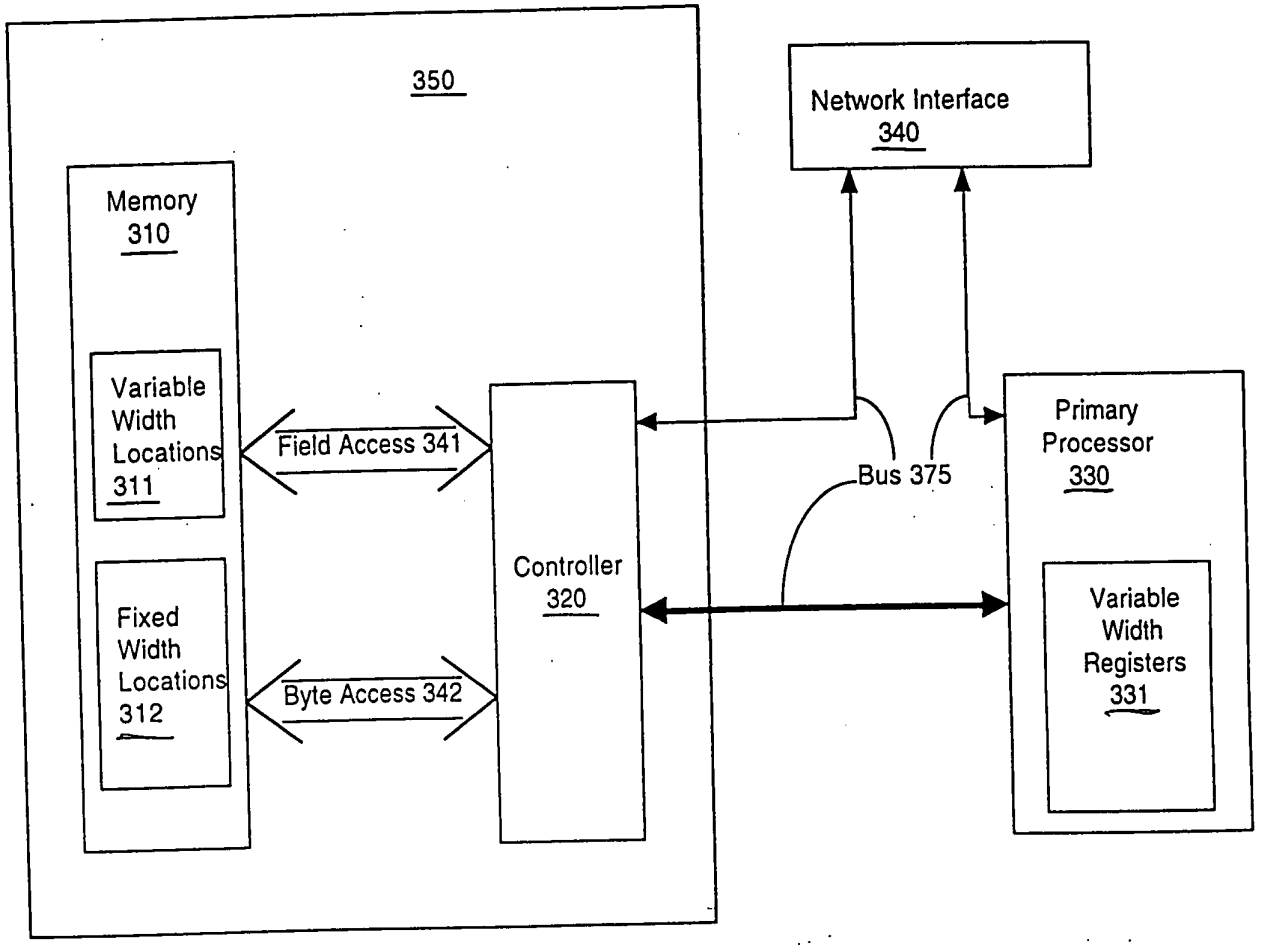
300
350
Network Interface
340
Memory
310
Variable
Width
Locations
311
Fixed
Width
Locations
312
Field Access 341
Byte Access 342
Controller
320
Bus 375
Primary
Processor
330
Variable
Width
Registers
331

FIG 3A

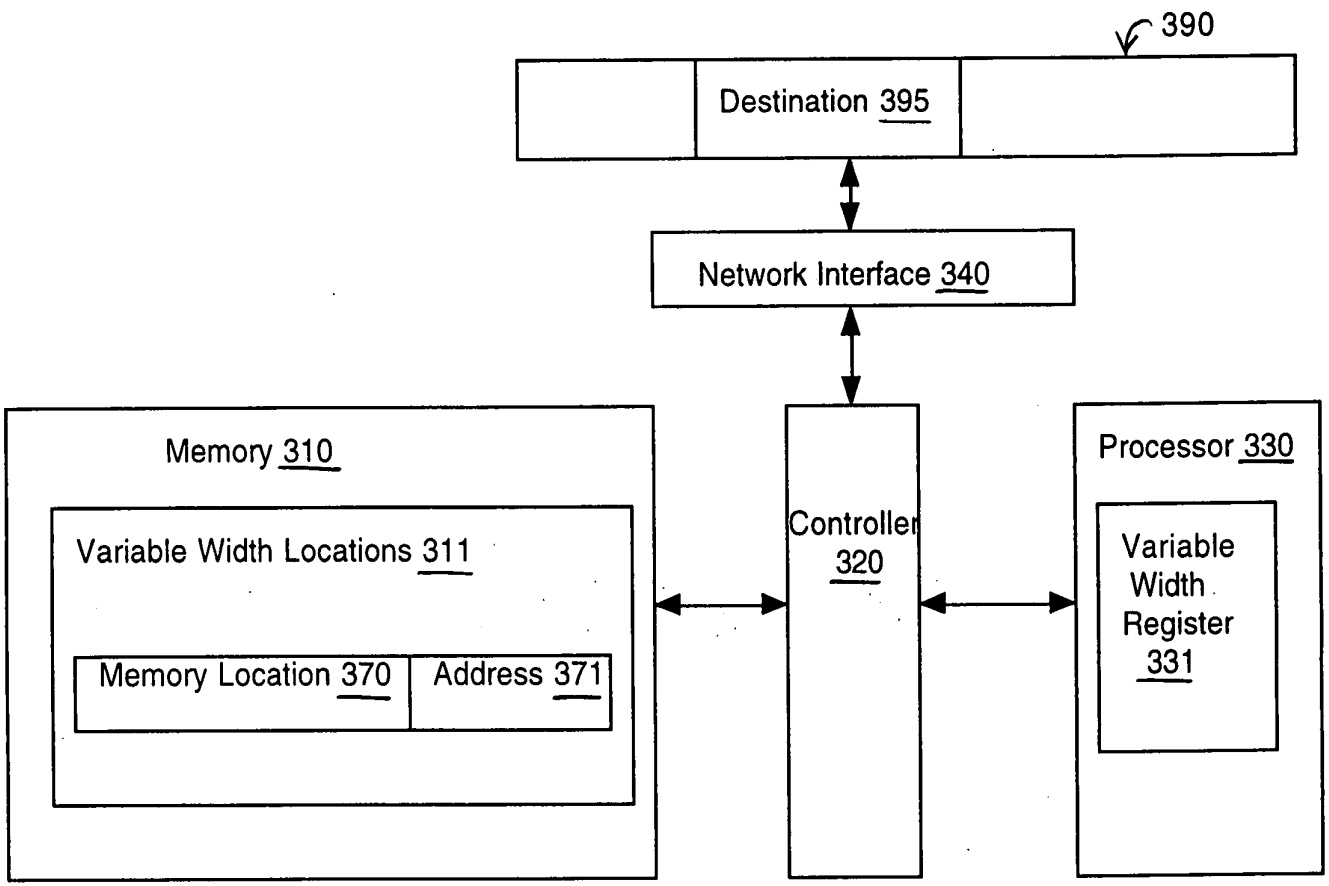
390
Destination 395
Network Interface 340
Memory 310
Variable Width Locations 311
Memory Location 370
Address 371
Controller 320
Processor 330
Variable Width Register 331

FIG 3B

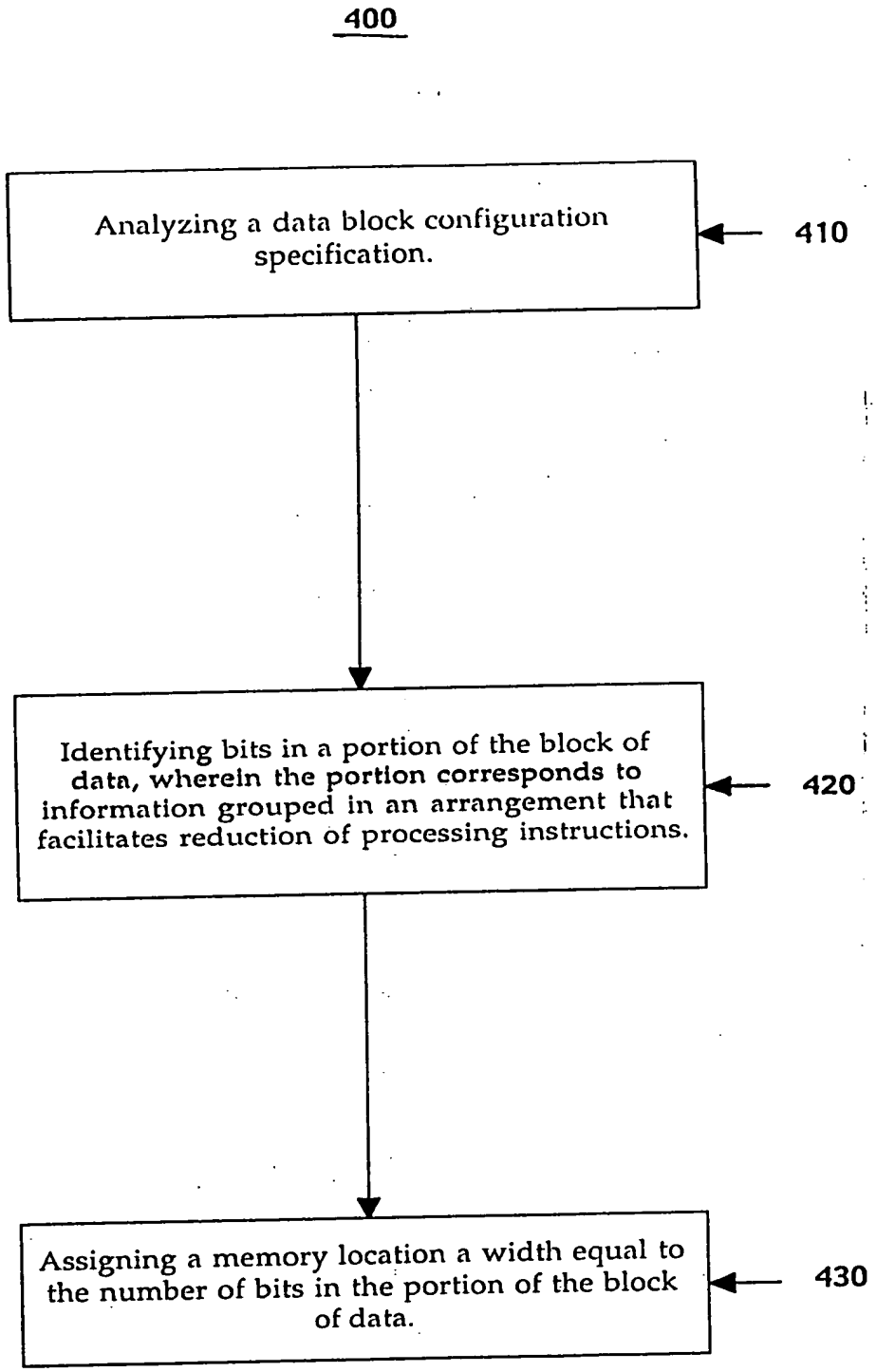
400
Analyzing a data block configuration specification.
410
Identifying bits in a portion of the block of data, wherein the portion corresponds to information grouped in an arrangement that facilitates reduction of processing instructions.
420
Assigning a memory location a width equal to the number of bits in the portion of the block of data.
430

FIG.4

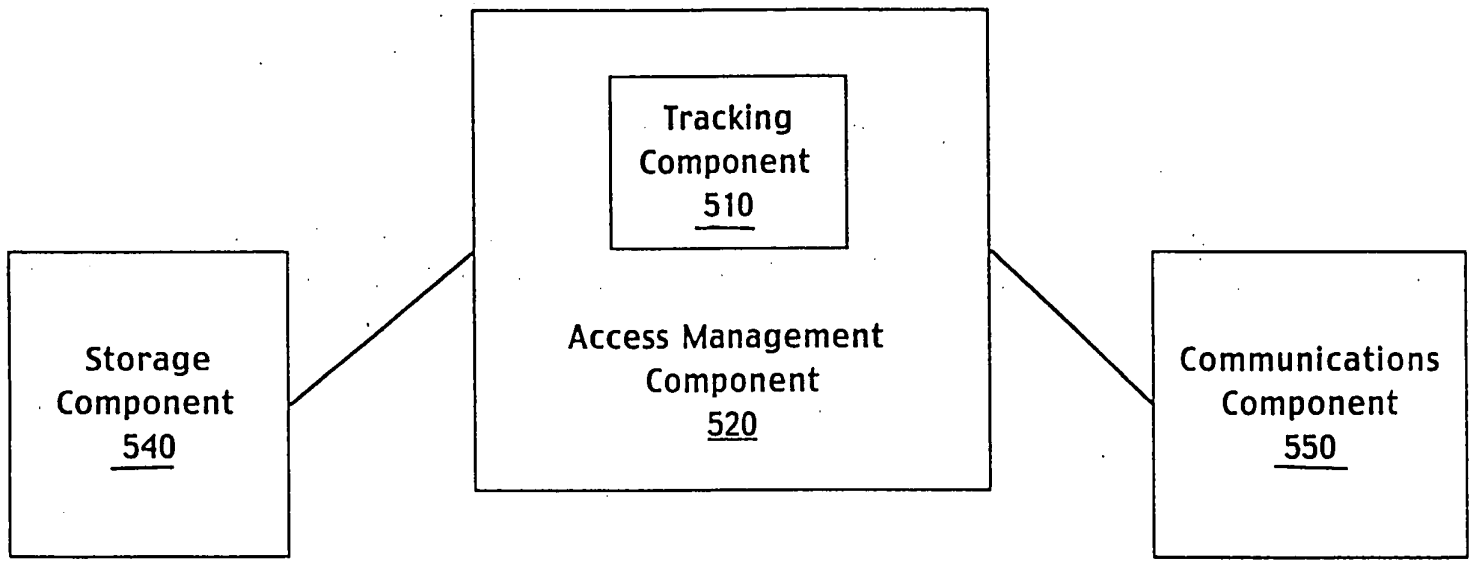
500
Tracking Component 510
Access Management Component 520
Storage Component 540
Communications Component 550

FIG. 5